ABSTRACT

A high-speed low-power dynamic current biased operational amplifier (Op-amp) for use in switched capacitor circuits. The system and method reduces current in the reset process of the switched capacitor circuit's operation, while maintaining the drive current required for fast settling in the amplification process. The system and method significantly lowers the power consumption of the switched capacitor circuit, while overcoming the main issues related to dynamic current biasing in an Op-amp, common-mode feedback interaction, using architecture other than the standard differential input stage of a normal Op-amp.